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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,686	10/23/2001	Ken-Ming Li	VIU.01-0001-US	7296

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
02/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO@HUFFMANLAW.NET

Office Action Summary	Application No.	Applicant(s)	
	10/032,686	LI ET AL.	
	Examiner	Art Unit	
	HUNG VU	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/20/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,34-52 and 57-68* is/are pending in the application.

4a) Of the above claim(s) *18-21,36-38,40-50 and 52* is/are withdrawn from consideration.

5)☒ Claim(s) *63-68* is/are allowed.

6)☒ Claim(s) *1-17,34,35,39,51,57,58,61 and 62* is/are rejected.

7)☒ Claim(s) *59 and 60* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/08/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Invention of Embodiment of Figure 3, Claims 1-17, 34-35, 39, 51, and 57-68 in the reply filed on 05/23/07 is acknowledged. The traversal is on the ground(s) that there is no giving reason why each invention is distinct and they would be a serious burden on the examiner. This is not found persuasive because there is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph..

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 18-21, 36-38, 40-50 and 52 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 05/25/07.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17, 34-35, 39, 51, 57-58 and 61-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao (PN 5,838,204, of record) in view of Nakamura (PN 6,476,505).

Regarding claims 1 and 57, Yao discloses, as shown in Figures 8-10, an integrated circuit comprising:

a power supply I/O pad (a portion of 606);

an I/O pad (another portion of 606) of a first type made of a deposited conductor, wherein the I/O pad (606) of the first type is connected to a first point on an integrated circuit;

and a strip (not shown, but inherently connect to the circuit) of deposited conductor substantially adjacent to the I/O pad (606) of the first type, wherein the strip of disposed conductor is connected to a second point on the integrated circuit.

Yao does not disclose the I/O pad of the first type is narrower than the power supply I/O pad so as to allow space for the strip. However, Nakamura discloses the I/O pad of the first type (2) is narrower than the power supply I/O pad (3) so as to allow space for the strip (4). Note Figures 1-3 and 6-15 of Nakamura. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made for the I/O pad of the first type of Yao being narrower than the power supply I/O pad, such as taught by Nakamura in order to allow space for the strip, to prevent the short circuit, and to provide more power to the device.

Regarding claims 2 and 58, Yao and Nakamura disclose the I/O pad (606) of the first type is a data I/O pad.

Regarding claim 3, Yao and Nakamura disclose the first point on the integrated circuit is further connected to a circuitry.

Regarding claim 4, Yao and Nakamura disclose the first point on the integrated circuit is further connected to a power bus (608).

Regarding claim 5, Yao and Nakamura disclose the second point on the integrated circuit is further connected to a circuitry.

Regarding claim 6, Yao and Nakamura disclose the second point on the integrated circuit is further connected to a power bus (608).

Regarding claims 7 and 61, Yao and Nakamura disclose the strip (another portion of 606) of conductor is connected to a third point on the integrated circuit.

Regarding claim 8, Yao and Nakamura disclose the second and third points on the integrated circuit are connected to a circuitry.

Regarding claim 9, Yao and Nakamura disclose the second and third points on the integrated circuit are connected to a power bus (608).

Regarding claim 10, Yao and Nakamura disclose an I/O pad (2) of the second type made of a conductor, wherein the I/O pad of the second type is connected to a third point on the integrated circuit;

a second strip (4) of conductor, wherein the second strip is located alongside the I/O pad of the second type, and wherein the second strip is connected to a fourth point on the integrated circuit;

wherein the I/O pad of the second type is narrower than the power supply I/O pad in order to make room for the second strip.

Regarding claim 11, Yao and Nakamura disclose the I/O pad (a next portion of the first type of I/O pad (606)) of the second type is a data I/O pad.

Regarding claim 12, Yao and Nakamura disclose the third point on the integrated circuit is further connected to a circuitry.

Regarding claim 13, Yao and Nakamura disclose the third pint on the integrated circuit is further connected to a power bus (608).

Regarding claim 14, Yao and Nakamura disclose the second strip (4) of conductor located alongside the I/O pad of the first type, wherein the second strip is connected to a third point on the integrated circuit, and wherein the I/O pad of the first type is narrower than the power supply I/O pad in order to make room for the strips of conductor.

Regarding claim 15, Yao and Nakamura disclose the second, third and fourth points on the integrated circuit are connected to a circuitry.

Regarding claim 16, Yao and Nakamura disclose the second, third and fourth points on the integrated circuit are connected to a power bus (608).

Regarding claim 17, Yao and Nakamura disclose the I/O pad (a portion of 606) of the first type provides power to a core circuitry (602).

Regarding claim 34, Yao discloses, as shown in Figures 8-10, an integrated circuit comprising:

a positive power supply I/O pad (a portion of 606) made of a deposited conductor;

a positive power bus (608) connected to the positive power supply I/O pad (a portion of 606);

a data I/O pad (another portion of 606) made of a deposited conductor; circuitry connected to the data I/O pad (other portion of 606);

a first strip (not shown, but inherently connect to the circuit) of deposited conductor substantially adjacent to the data I/O pad, wherein the strip of deposited conductor is connected

to multiple points (multiple points portions of another portion of 606) on the positive power bus (608); and

It is inherent that a negative power supply I/O pad, a negative power bus, and a second strip made of a deposited conductor will be the same as those for the positive power because they will provide a negative power supply I/O and positive power supply I/O for the operation of the circuit.

Yao does not disclose the I/O pad is narrower than the power supply I/O pads so as to allow space for the strips. However, Nakamura discloses the I/O pad (2) is narrower than the power supply I/O pads (3) so as to allow space for the strips (4). Note Figures 1-3 and 6-15 of Nakamura. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made for the I/O pad of Yao being narrower than the power supply I/O pad, such as taught by Nakamura in order to allow space for the strips, to prevent the short circuit, and to provide more power to the device.

Regarding claim 35, it is inherent that the power buses (608) of Yao and Nakamura provide positive and negative power to a core circuitry (602).

Regarding claims 39 and 51, Yao and Nakamura disclose the I/O pad (606) is a data I/O pad.

Regarding claim 62, it is inherent that the strip connected to the power buses (608) of Yao and Nakamura, wherein the power bus is configured to provide power to a core circuitry (602) of the integrated circuit.

Allowable Subject Matter

4. Claims 59 and 60 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 63-68 are allowed.

6. The following is an examiner's statement of reasons for allowance:

Applicant's claims 59-60 and 63-68 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed circuit comprising the strip of conductor being positioned on an outer portion of the I/O pad, as recited in claim 59; the conductor forming the metal contact is positioned on an inner portion of the I/O pad and the strip of conductor is positioned on an outer portion of the I/O pad, as recited in claim 60; a pad comprising at least a first portion and a second portion, wherein the first portion of the pad includes an I/O pad of a first type made of a conductor connected to a first point on the integrated circuit, a second portion includes a strip of conductor located alongside the I/O pad of the first type, the strip is connected to a second point on the integrated circuit, the I/O pad of the first type is narrower than the power supply I/O pad in order to make room for the strip, in combination with the remaining claimed limitations of claim 63.

Response to Arguments

7. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Monday to Thursday 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272 - 1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vu

January 31, 2008

Hung Vu

Primary Examiner